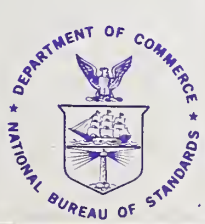
C CE & TECHNOLOGY:

IMPACT OF CHARGE-TRANSFER DEVICE TECHNOLOGY ON COMPUTER SYSTEMS



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COMPUTER SCIENCE & TECHNOLOGY:

Impact of Charge-Transfer Device Technology on Computer Systems

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PREFACE

"Charge-transfer device" is a generic term that can be applied to a family of several types of integrated silicon devices -- this document describes two such devices - the bucket-brigade device and the charge-coupled device. Technical and economic aspects of charge-transfer device research are addressed and compared. Conclusions are presented which suggest future impacts of charge-transfer devices on current electronic systems, especially computers. Capabilities and accomplishments of charge-transfer device research facilities in Japan, Canada, Great Britain, The Netherlands, the Federal Republic of Germany, and the United States are described.

Information contained in this report was derived from the open technical literature and from private interviews with various U.S. technical experts. Where possible, references in the open literature are cited, although the opinions of technical experts were checked in order to substantiate the salient points.

The technology assessment resulting in this report was conducted by the Information Technology Division of the Institute for Computer Sciences and Technology, National Bureau of Standards, as part of an "Advanced Computer Technology Survey" project. Mr. Robert B. J. Warnar was the principal technical investigator and was responsible for the preparation of this report. He was assisted by Mr. Peter J. Calomeris. NBS technical consultants who contributed significantly were: Dr. Martin G. Buehler and Mr. Robert I. Scace, both of the Electronic Technology Division, Institute for Applied Technology; and Mr. Sidney B. Geller of the Computer Engineering Division, Institute for Computer Sciences and Technology. Mr. Edwin J. Istvan, Acting Chief of the Information Technology Division, and Mr. George E. Lindamood, project leader, provided editorial assistance.

CONTENTS

Page

Note iii

Preface v

Abstract 1

1. Charge-Transfer Device Overview 1

Charge-Transfer Devices 1
Principles of Operation of Charge-Transfer Devices 1
Charge-Transfer Device Electrode Structures 8
Technical Obstacles in Charge-Transfer Devices 10
Charge-Transfer Device Applications 10
Charge-Transfer Device Computer Application Trends 11
CCD Computer Main Frame Memories 12
CCD Computer Swap Memories 12
CCD Computer Mass Memories 12

2. Charge-Transfer Device Parameters 14

Bit-Storage Densities of Charge-Transfer Devices 14
Charge-Transfer Efficiency of Charge-Transfer Devices 14
Charge-Transfer Device Data Rates 14
Charge-Transfer Device Power Dissipation 19
Charge-Transfer Device Prices 19

3. Non-U.S. Charge-Transfer Device Technology 22

CTD Technology in Canada 22
CTD Technology in The Netherlands 23
CTD Technology in Japan 26
CTD Technology in Great Britain 27
CTD Technology in The Federal Republic of Germany 28

4. Summary and Conclusions 29

5. Glossary 32

Glossary of Terms Applicable to Charge-Transfer Devices 32
Glossary of Memory Terms 34

6. References 35

LIST OF FIGURES

Page

Figure 1 - Simplified Charge-Transfer Device Equivalent Circuit 2
Figure 2 - The Discrete MOSFET Model of a Charge-Transfer Device 2
Figure 3 - Phase 1 - Mechanical Analogy of a Charge-Transfer Register 3
Figure 4 - Phase 2 - Mechanical Analogy of a Charge-Transfer Register 3
Figure 5 - Phase 3 - Mechanical Analogy of a Charge-Transfer Register 4
Figure 6 - The Charge-Coupled Device Storage Element. 4
Figure 7 - Charge Storage in a Charge-Coupled Device During Phase 1 5
Figure 8 - Three-Phase Clock Signals for Charge-Coupled Device. 5
Figure 9 - Charge Transfer in a Charge-Coupled Device During Phase 2. 5
Figure 10a - Input-Diode Electron Injection 6
Figure 10b - Avalanche Electron Injection in a Charge-Coupled Device 7
Figure 10c - Electron Injection by Light in a Charge-Coupled Device 7
Figure 11 - Output-Diode Data Detection in a Charge-Coupled Device. 7
Figure 12 - Charge-Coupled Device 8
Figure 13 - Bucket-Brigade Device 8
Figure 14a - Surface-Channel CCD. 8
Figure 14b - Buried-Channel CCD 8
Figure 15 - Construction of the Peristaltic Charge-Coupled Device 9
Figure 16 - Nonoverlapping Electrode 3ϕ CCD 9
Figure 17 - Overlapping Electrode 4ϕ CCD. 9
Figure 18 - CCD Computer Memory Application Trends. 11
Figure 19 - Bit-Storage Densities of Charge-Transfer Devices. 15
Figure 20 - Charge Transfer Efficiency of Charge-Transfer Devices 16
Figure 21a,b - Charge-Transfer Device Data Rates. 17, 18
Figure 22 - Power Dissipation of Charge-Transfer Devices. 20
Figure 23 - Charge-Transfer Device Prices 21
Figure 24 - Castellated CCD Structure 22

LIST OF TABLES

Page

Table 1 - Developments in Memory CCD's (1975-1978). 13

Table 2 - Charge-Transfer Device Technological Accomplishments in The Netherlands and the United States 25

Table 3 - Technological Accomplishments of Non-U.S. and U.S. CTD Facilities (through 1975). 30

IMPACT OF CHARGE-TRANSFER DEVICE TECHNOLOGY ON COMPUTER SYSTEMS

Robert B. J. Warnar

ABSTRACT

This document assesses the status of charge-transfer device technology as displayed by foreign research and manufacturing facilities for a period up to September 1975. Capabilities and accomplishments of charge-transfer device research facilities in Japan, Canada, Great Britain, The Netherlands, The Federal Republic of Germany, and the United States are described. Technical and economic factors are addressed and compared. Conclusions are presented which suggest future impacts of charge-transfer devices on current electronic systems, especially computers. Information contained in this report was derived from the open technical literature and from interviews with various U.S. technical experts. The technology assessment resulting in this report was conducted by the Information Technology Division of the Institute for Computer Sciences and Technology, National Bureau of Standards, as part of an "Advanced Computer Technology Survey" project.

Key words: Bucket-brigade; buried channel; Canada; charge-coupled device; Great Britain; imager CCD's; Japan; peristaltic CCD's; surface channel; The Federal Republic of Germany. The Netherlands; transfer channel;

1. CHARGE-TRANSFER DEVICE OVERVIEW

Charge-Transfer Devices

A device whose operation depends on the movement of discrete packets of charge along or beneath a semiconductor surface is called a charge-transfer device (CTD). The first fully integrated metal-oxide-semiconductor CTD, the bucket-brigade device, was developed in 1969 by F. L. J. Sangster (U.S. patent 3,546,490), NV Philips Gloeilampenfabrieken in The Netherlands, while W. S. Boyle and G. E. Smith from Bell Telephone Laboratories, are credited with the first U.S. version of a CTD, the charge-coupled device (CCD). [1] [1]

More recently, L. J. M. Esser, another Philips scientist [2], noted that in charge-transfer devices, the transfer speed and efficiency are determined primarily by the transport of the last fraction of each charge packet. Accordingly, he developed the peristaltic charge-coupled device (PCCD), in which the transport of the last fraction of charge of each packet is performed more efficiently than in the conventional CCD. [2]

Charge-transfer devices are clocked in order to move the charge packets. Single or multiple-phase clocking can be used. [3, 4, 5]

Principles of Operation of Charge-Transfer Devices (Bucket-Brigade and Charge-Coupled Devices)

The theory of charge-transfer devices was first proposed by U.S. engineer K. Schlesinger (U.S. patent 2,403,955) in the 1940's, but integrated circuit versions of CTD designs, such as charge-coupled devices and bucket-brigade devices, did not occur until the late 1960's and early 1970's. [6]

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[1] Figures in brackets indicate the literature references on page 35.

The theory of the charge-transfer device was based on the idea that the simplest mode of storing information is as a charge on a capacitor. In addition, this charge must be transferred easily and efficiently from its location to a destination where the charge can be translated into meaningful data. Individual capacitors must, therefore, be connected together with switches that alternately open and close in order to transfer the individual charges (see Figure 1).

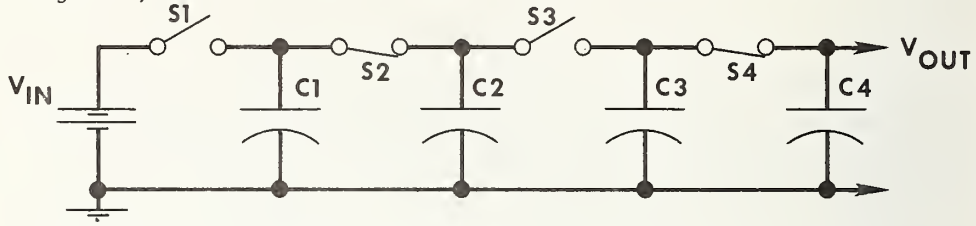

Figure 1: Simplified Charge-Transfer Device Equivalent Circuit

The above simplified circuit of a discrete charge-transfer device is characteristic of an analog delay line or a serial shift register. Operation commences when switch S1 is closed while S2 is open and C1 is charged to potential Vin. After a period of time S1 is opened and S2 is closed (S3 is open). Part of the charge of C1 is now transferred to C2. Some time later, S2 is opened and S3 is closed (S4 is open). At this time some of the charge of C2 is transferred to C3. Finally, S3 is opened and S4 is closed--some charge of C3 is now transferred to the output capacitor C4. A more efficient operation of this model occurs when S1 and S3 are positioned simultaneously in one direction while S2 and S4 are placed in the opposite position. One soleniod could therefore operate S1 and S3 while the other positions S2 and S4. Such an operation is called a two-phase approach and this system is found in current CTD's. It should be noted that part of the charge is always left behind during each transfer--this obstacle is evident in the ensuing description of CTD's.

Krause in 1976 [1] applied the charge transfer principle to a transistor/capacitor shift register and, Langster and Teer in 1969 [1] applied the theory subsequently to metal-oxide-semiconductor field-effect transistors (MOSFET) as shown in Figure 2.

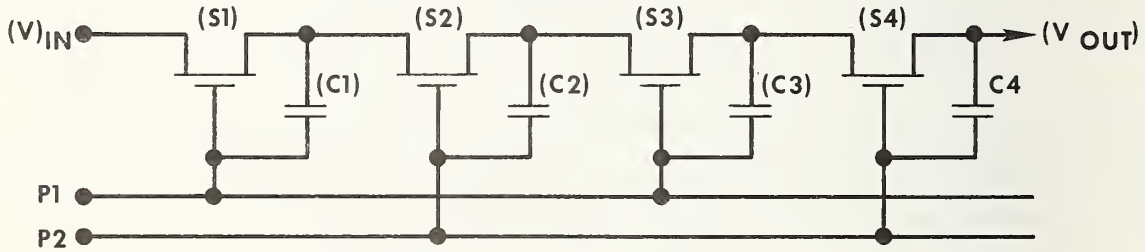

Figure 2: The Discrete MOSFET Model of a Charge-Transfer Device [1]

The characteristic low "on" resistance and high "off" resistance of MOSFET's S1, S2, S3, and S4 combined with their relatively good frequency response makes the above circuit a practical device--whose operation is as easily understood as that of the circuit in Figure 1. The MOSFET circuit was eventually called the bucket-brigade device (BBD) and is characterized by the fact that it uses the equivalent of one transistor and one capacitor per stage.

Following a different route, Bell Laboratories' Boyle and Smith [1] suggested that closely-spaced capacitors on an isolated surface of a semiconductor would serve to store and transfer electrical charges. These electrodes, closely spaced from each other at micrometer distances would, when pulsed with proper potentials and waveforms, generate "moving potential wells" carrying packets of charge. [1]

G. A. Amelio (see reference 59) was able to provide a dramatic representation of such a system (see Figure 3, 4, and 5).

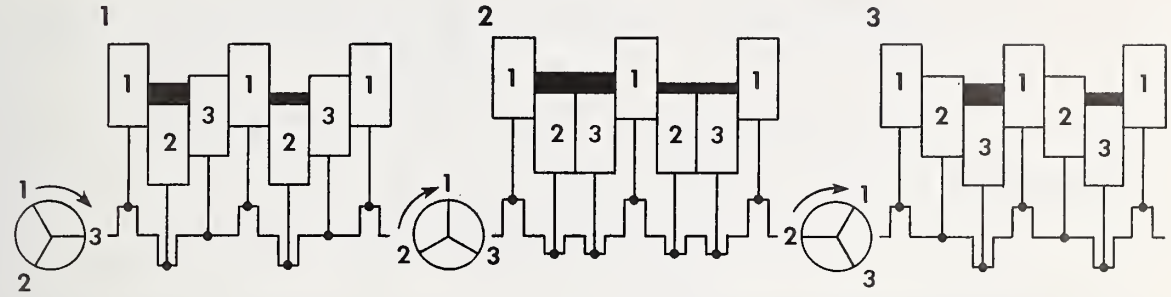

Figure 3: Phase 1 - Mechanical Analogy of a Charge-Transfer Register

Amelio visualizes the operation of the charge-transfer register as the operation of a machine that consists of a repeating series of three reciprocating pistons with a crankshaft and connecting rods to drive them. The dark areas in part 1 of Figure 3 are fluids and are analogous of charge packets in charge-transfer devices. The crankshaft can be turned either clockwise or counterclockwise. In the example, it is assumed that the crankshaft turns in a clockwise manner. During this period, number 2 pistons rise while number 3 pistons drop down (part 2). In part 3 of the Figure, all of the fluid is transferred to the top of the number 3 pistons. The presentation is extremely graphic even to the point that some fluid remains behind as it "sticks" to the top of pistons which defect is analogous to the charge loss in charge-transfer devices.

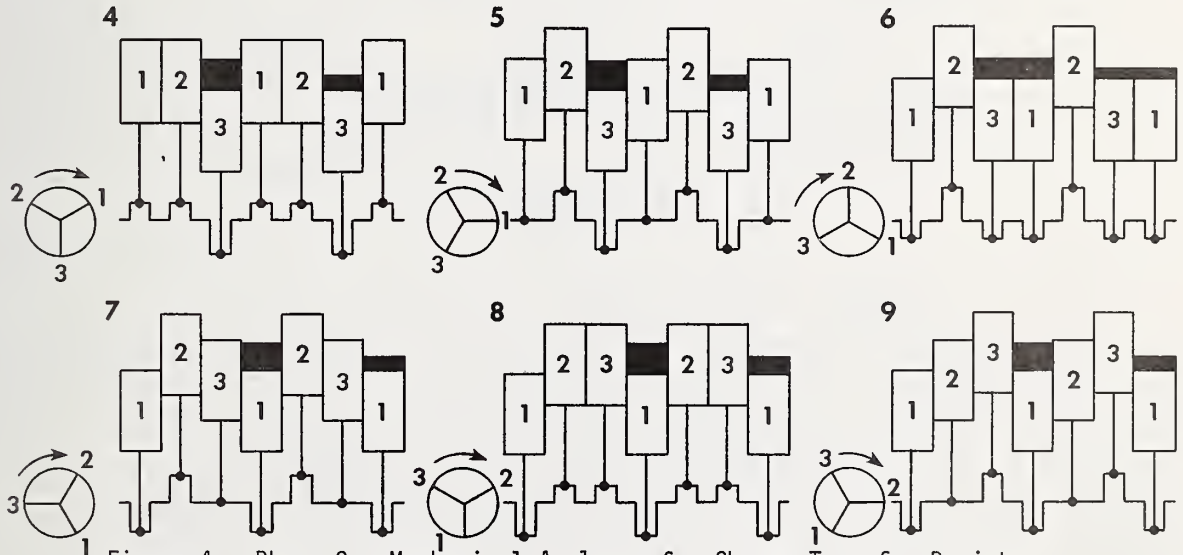

Figure 4: Phase 2 - Mechanical Analogy of a Charge-Transfer Register

Continuous clockwise rotation of the crankshaft transfers the fluid to the number 1 pistons thereby concluding phase 2 of the operation.

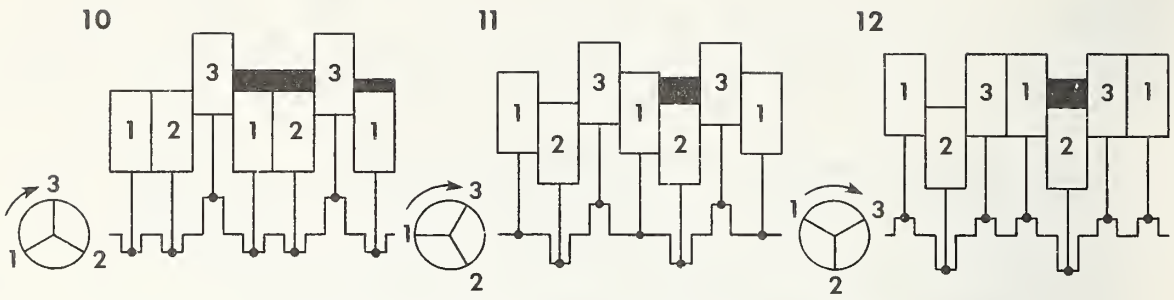

Figure 5: Phase 3 - Mechanical Analogy of a Charge-Transfer Register

The final cycle, phase 3, is shown in Figure 5. The fluid is transferred from the number 1 pistons to the number 2 pistons (in the case of the charge-transfer register, from one storage cell to the next). The mechanical fluid transfer system is therefore called a three-phase system.

It should be noted that the crankshaft could have been turned in the counterclockwise direction. In this case, the fluid would be transferred from the right to the left, or oppositely from the example. The reverse operation should also hold true for symmetrical charge-transfer registers. However, little information was found in the available literature on this characteristic even though other types of silicon device registers are not fully capable of bi-directional operation.

Figure 6 is a storage element of a charge-coupled device.

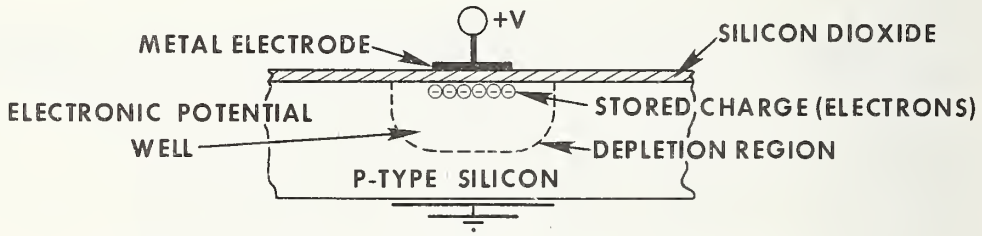

Figure 6: The Charge-Coupled Device Storage Element

A metal electrode is applied to a silicon substrate (P-type silicon in this case). The metal, usually aluminum, is separated from the substrate by a thin layer of silicon dioxide (SiO_2). When a potential (+V) is applied between the electrode and its substrate, electrons accumulate near the upper surface of the silicon beneath the electrode. When the source of potential is disconnected, the electrons remain under the electrode; but, the charge is reduced in time primarily due to electrical leakage through the large but still finite resistance of the SiO_2 layer. This loss of charge is characteristic of dynamic memories. The charge loss introduces the requirement for periodic replacement of the lost charges. Commonly, this cycle is called the "refresh cycle" in dynamic memories of which charge-transfer devices are members. The region under the upper metal electrode that is occupied by electrons, and is void of holes, is referred to as the depletion region. In general, the capacitance of the above storage element is somewhere near 0.1 picofarads. When the charge, about 1.5 picocoulombs, is transferred from one element to the next, the output signal current is 0.5 microamperes at speeds of around 1 megahertz.

Figure 7 shows a three-phase charge-coupled device with a charge-packet under the Ø1 electrode.

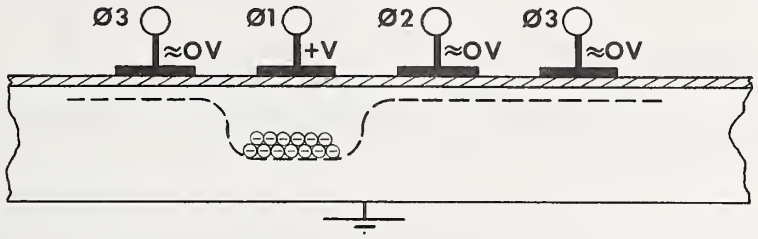

Figure 7: Charge Storage in a Charge-Coupled Device during Phase 1

Since electrons are collected under the Ø1 electrode, a potential approaching the device supply voltage (+V) exists between the Ø1 electrode and ground. The other electrodes exhibit a near 0 volt potential at this time (t1) as shown in Figure 8.

In order to move the charge from the Ø1 to Ø2 electrode position, an electric potential well has to be introduced under the Ø2 electrode while at the same time the Ø3 electrode potential well must repel the Ø1 electrons. This operation is accomplished by the use of the following three-phase clock wave forms (Figure 8).

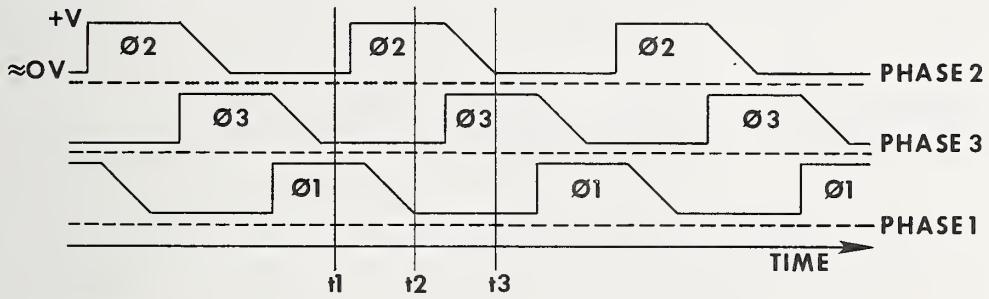

Figure 8: Three-Phase Clock Signals for Charge-Coupled Device

Time t1 in the above timing diagram is chosen as a starting point. This is the condition of the CCD in Figure 7.

As time progresses, toward the right, the next positive pulse occurs in Ø2 (at time t2). The condition of the CCD example is now as shown in Figure 9.

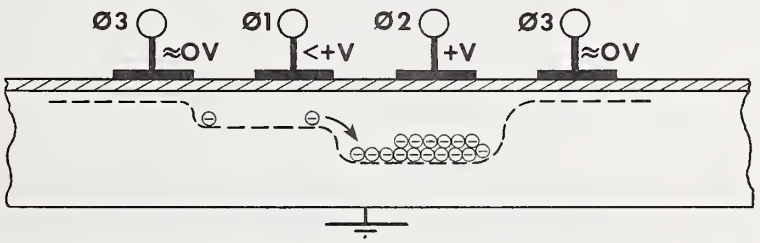

Figure 9: Charge Transfer in a Charge-Coupled Device during Phase 2

At the conclusion of phase 2, all of the electrons should be transferred to a position under electrode Ø2.

It should be noted that during the phase 2 transfer period, the Ø3 wells on either side of the charge packets are very shallow. The Ø3 wells therefore act like very high impedance paths for the electrons and therefore confine the electrons in the Ø1 and Ø2 wells. This is the major reason for using the described 3 phase transfer operation--it provides charge packet isolation.

No amplification of signal is present during the process. Due to this fact and other factors such as thermal, time, and trapping considerations, losses of electrons occur. These losses are expressed in terms of transfer efficiency. The transfer efficiency of a charge-transfer device can be defined as the fraction of a charge packet that is transferred completely and is shown later to be in the range of 98.00% to 99.999% per stage.

The next positive pulse to be encountered in time is the phase 3 pulse. The potential of the phase 2 clock is rapidly declining during this period (the charge packet, however, remains intact). Most of the electrons are now moved to and are positioned under the phase 3 electrode.

Thus far, only the transfer of charge packets has been discussed. The following sections will now explain how electrons are "injected" into and "extracted" from the CCD arrays.

Several methods are used to introduce signal levels into CCD arrays; the most common techniques are the following:

Injection diode
Surface avalanche
Light projection

Figures 10a, b, and c show the different techniques of signal introduction to the CCD array.

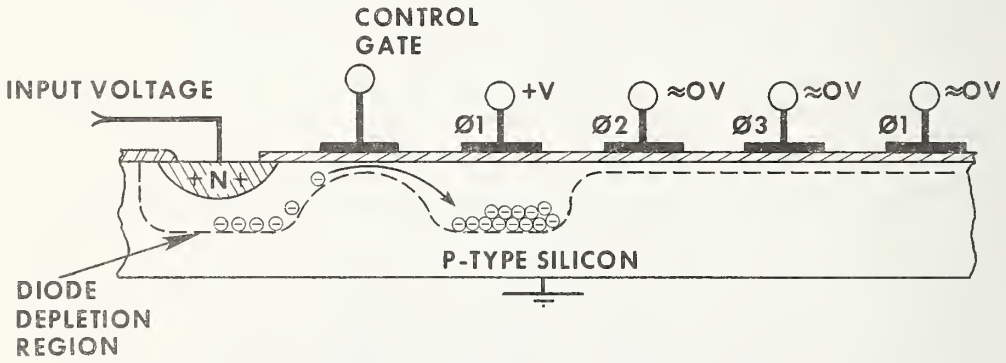

Figure 10a: Input-Diode Electron Injection

Electrons are injected under the control of both the diode (P-N) and the Control Gate. The diode acts as an infinite source of minority carriers, or electrons, in this case. As the electrons appear in the depletion region under the diode, the Control Gate "funnels" this charge to the Ø1 electrode at the Ø1 clock period.

Figure 10b shows the avalanche injection method.

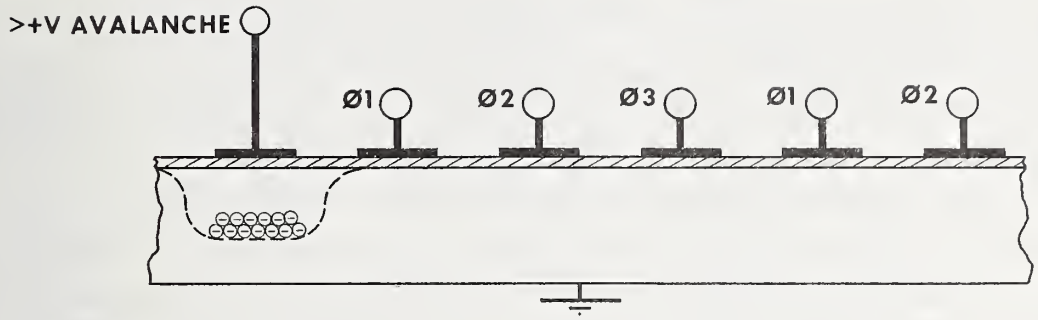

Figure 10b: Avalanche Electron Injection in a Charge-Coupled Device

Electrons are injected into a well under the +V *avalanche* electrode by a high potential that is applied to this electrode. The potential is much greater than the clock potentials +V (clocking potentials are set at such levels as not to introduce distortion in the stored information). The quantity of introduced electrons is thus related to the amplitude of +V *avalanche*.

Figure 10c is a schematic diagram of a solid-state charge-coupled device image sensor.

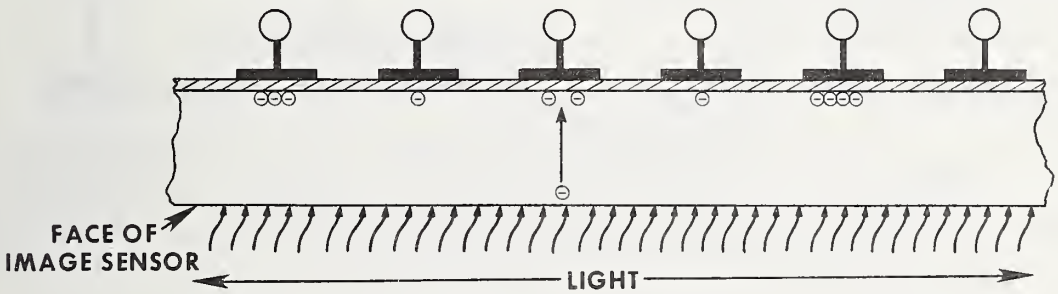

Figure 10c: Electron Injection by Light in a Charge-Coupled Device

Electrons are introduced to the various electrodes of the image sensor by the amount of light that is received on the side, or face, opposing the electrode structures. The greater the amount of light on the face of the device, the more electrons are introduced per unit area as is shown in Figure 10c. The collected charges under the electrodes are thus an analog replica of the light pattern impinging on the lower side of the charge-coupled device sensor. These charges can be scanned by the described clocking methods and can be detected as trains of wave forms, the amplitudes of which are directly proportional to the gray scale of the image. The array can therefore be called self-scanning, and is an analog application of the charge-coupled device.

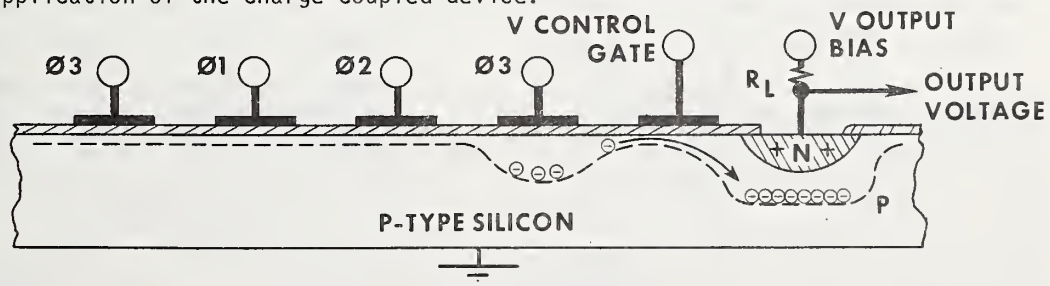

Figure 11: Output-Diode Data Detection in a Charge-Coupled Device

Figure 11 shows a means of charge, or data, detection for a charge-coupled device. This method is used almost universally and depends upon the characteristics of the reverse biased diode (the P-N junction in Figure 11). In addition, an output gate electrode structure is installed to reduce the clock signal effect on the data as they are presented to the P-N diode. Detection of data proceeds as follows; at the end of Ø3, the charge to-be-detected is located under the Ø3 electrode. When the Ø3 clock signal starts approaching the ground voltage, the charge is passed by the output gate and is collected by the P-N diode. The collection of the electrons under the diode causes a current to flow in the load resistor R_L, which in turn produces the desired output voltage, or data signal.

Charge-coupled devices and bucket-brigade devices are relatively similar in operation.

In both bucket-brigade devices (BBD's) and charge-coupled devices (CCD's), packets of charge carriers are moved around beneath the surface of a semiconductor crystal without a direct electrical connection to the crystal. The carrier packets are manipulated by means of localized electric fields called "potential wells," that are controlled by potentials applied to electrodes that are deposited on a thin insulating layer at the semiconductor (usually silicon) surface. But, whereas the CCD uses a completely homogeneous crystal and relies upon potential wells which are induced into the lattice to hold the carriers together as a packet (see Figure 12), the BBD uses wells of opposite impurity doping which are deposited on the main crystal (see Figure 13). [7, 8, 9, 10]

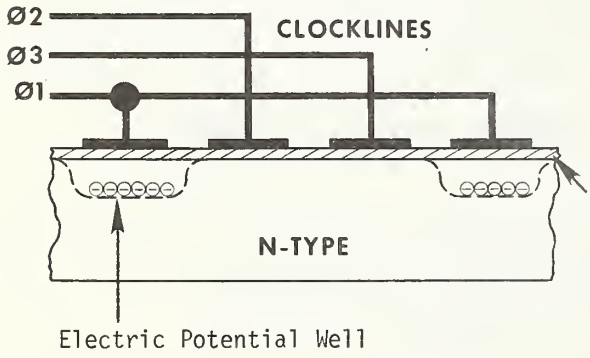

Figure 12: Charge-Coupled Device

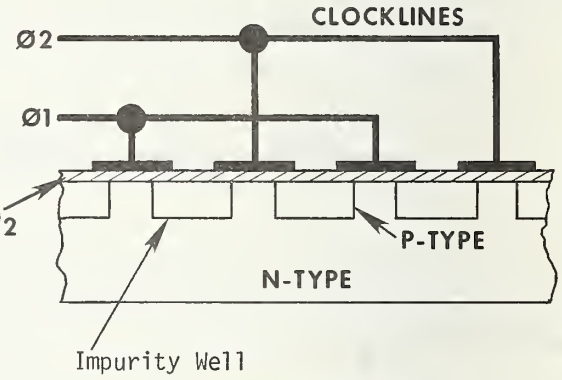

Figure 13: Bucket-Brigade Device

Charge-Transfer Device Electrode Structures

Bucket-brigade devices from various manufacturers all appear to be constructed by using similar methods. CCD's, on the other hand, are constructed with a greater variety of structures. Generally speaking, two types of CCD's are noteworthy:

The Surface-Channel CCD (see Figure 14a) [11]
The Buried-Channel CCD (see Figure 14b) [12, 13, 14]

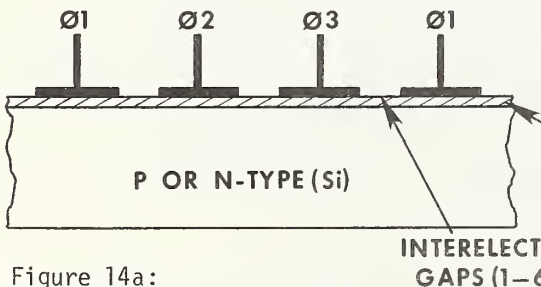

Figure 14a:
Surface-Channel CCD (SCCD)

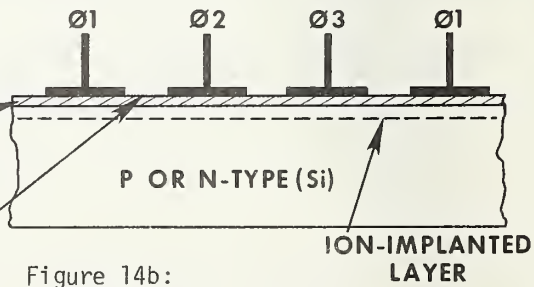

Figure 14b:
Buried-Channel CCD (BCCD)

The surface-channel CCD (SCCD) appeared on the scene first. It suffered from poorer transfer efficiencies when compared to more recent buried-channel devices which can operate at higher frequencies and which are relatively free of loss mechanisms such as surface recombination. This disadvantage of the SCCD is due to interactions of the signal carriers with conditions presented by the surface of the device. In other words, the channel charge is exposed to the Si-SiO_2 interface where interface states cause charge recombinations resulting in poorer transfer efficiencies. [11]

The peristaltic charge-coupled device (PCCD) is a special type of buried-channel charge-coupled device (BCCD). As in all BCCD's, the effect of surface states on the charge transfer efficiency can be greatly reduced by operating in the buried channel mode (see Figure 14b). In the PCCD, increased efficiency is obtained by introducing two or more layers (instead of one layer as other types of BCCD's) between the substrate and the surface of the crystal (see Figure 15). [15]

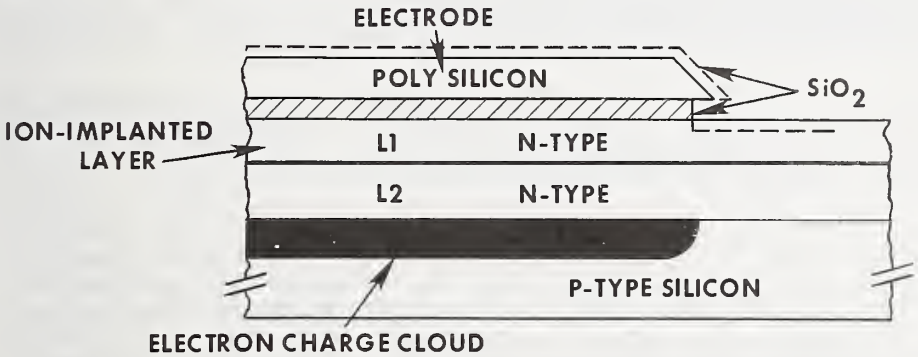

Figure 15: Construction of the Peristaltic Charge-Coupled Device

In this Figure, layer number one (L1) is an ion-implanted layer that is placed on top of the N-type epitaxial layer L2. Both layers rest on the P-type silicon substrate. The net effect of the double layer is to keep the charge cloud farther away from the surface of the device, thereby preventing surface charge recombination. The extra layer construction insures a low charge loss and thereby a high charge-transfer efficiency for the PCCD. [16]

Many CCD manufacturers desiring advanced CCD operating characteristics, are dropping the SCCD design and are presently developing BCCD's. Other CCD manufacturers, however, will continue to use SCCD construction since the SCCD fabrication process is less costly than either the BCCD or PCCD.

The attachment and position of the CCD electrodes are vital to the operation of charge-transfer devices. Several methods for electrode attachment are used, but most CTD electrodes are fabricated by aluminum or polycrystalline silicon deposition. Interelectrode structures are usually one of two types: [16, 17] (see Figure 16 and Figure 17 [18, 19])

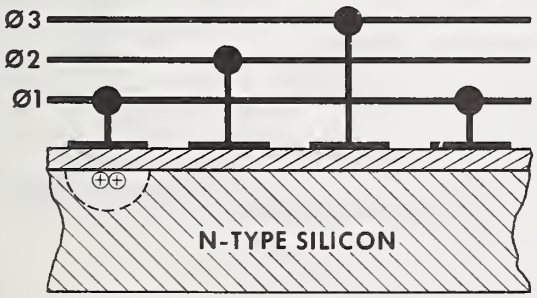

Figure 16:
Nonoverlapping Electrode 3Ø CCD

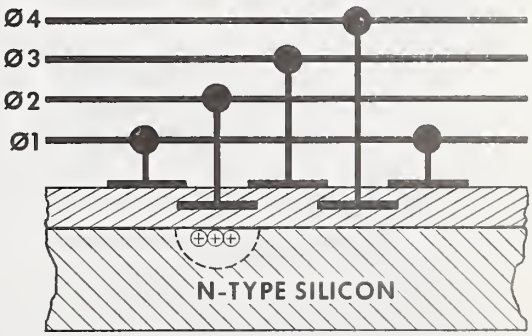

Figure 17:
Overlapping Electrode 4Ø CCD

In nonoverlapping gate structure design, the distance between the electrodes has a great effect on the device transfer efficiency and high frequency operation. The minimum interelectrode gap distances are usually determined by the fabrication limits of the photolithographic process of the manufacturer in question. Thus, the better the lithographic process of the manufacturer, the smaller the CCD gaps. Most current CCD's use the overlapping gate design. [18, 20]

Technical Obstacles in Charge-Transfer Devices

Charge-transfer devices present a number of technical obstacles to the solid-state device and equipment manufacturer: [21, 22, 23, 24, 25]

Volatility (complete loss of data with loss of power supply voltage)
Bit-Serial Operation (slow access time)
Poor Charge-Transfer Efficiency (partial signal loss)
Poor Radiation Resistance (signal distortion or loss)
Current Photolithographic Limits (leading to CCD production yield problems)

It is doubtful whether the obstacles of poor radiation resistance and imcomplete charge transfer will ever be fully surmounted. However, the effects of these obstacles have little influence on the operation of currently-used commercial devices. These obstacles become important only in highly-specialized military applications. [21, 26, 27, 28]

The problems of volatility and bit-serial operation have some impact upon commercial CTD products. The volatility of the CTD is a factor to consider when choosing between CCD's and magnetic memories while the bit-serial operation influences the choice between CCD's and current random-access-memories (RAM). It is anticipated that a certain degree of nonvolatility will be attained in future CCD's through the use of metal-nitride-oxide (MNOS) circuitry. [29] Complete random access to any bit in a CCD memory is regarded by most scientists to be far more difficult.

Many U.S. manufacturers utilize conventional photolithographic techniques in producing CTD's. If higher CTD storage densities are going to be required, very expensive scanning electron-beam or X-ray lithographic equipment will be necessary. Another method which can be utilized to produce higher bit-capacity CTD chips at reasonable yields, is to introduce larger chips, thereby relaxing the demands on conventional photolithographic processing. At present only some U.S. companies are capable of producing large (up to 12 millimeter and larger on a side) silicon chips. [1, 21, 30]

Charge-Transfer Device Applications

The charge-transfer device is probably one of the most versatile solid-state LSI products that has been intented. New applications of charge-transfer devices, in the from of either BBD's, CCD's, or PCCD's, are still occurring. The following list identifies most of the applications of the charge-transfer device proposed to date:

Computer Oriented CCD Memories [31, 32, 33, 34]
Optical CCD Sensors [35, 36, 37, 38, 39]
Digital and Analog CCD and BBD Shift Registers [40, 41]
Moving-Target-Indicator Filters for Radar Systems [42, 43]
Nonvolatile MNOS CCD Memories [29]
Disk and Drum Replacement CCD Peripheral Memories [41, 44]
BBD Speech Compressors in Audio Equipment [45]
BBD Tremolo, Vibrator, and Choral Effect Control in Electronic Musical Instruments [46]
BBD Telephone Time Compressors and Voice Scramblers in Communication Systems [46, 47]
BBD Matched Filters [48]
CCD Integrated Imagers [30]
CCD Low Light Level Image Sensors [30]

Nonrecursive CCD Filters [50]
CCD Signal Processors [40, 51]
CCD Multiplexers and Demultiplexers [40, 41]

It is clear from the preceding list that charge-transfer devices can have a significant technological impact on digital and analog systems. It is also clear from current, researched literature that CTD's are still in the developmental process and require additional development to further reduce ill effects of certain inherent characteristics (such as volatility and charge-transfer inefficiency). The effort involved in overcoming these undesirable characteristics will be intense and highly competitive since the process is stimulated by the potential of creating a promising low-cost, versatile solid-state product. [21, 40]

Charge-Transfer Device Computer Application Trends

Of the devices presently recognized as charge-transfer devices, the technology most often applied to computer memory applications by both U.S. and foreign manufacturers is the CCD technology. Applications of CCD's fall into the following categories: [1, 52]

CCD Peripheral Mass Memories
CCD Swap Memories

Figure 18 shows how CCD's might have impact on computer memory systems. The figure is divided into three sections: [1, 53]

Computer Main Memories
Computer Swap Memories
Computer Peripheral Memories

Currently, CCD memories can perform well in the computer mass memory area. [44]

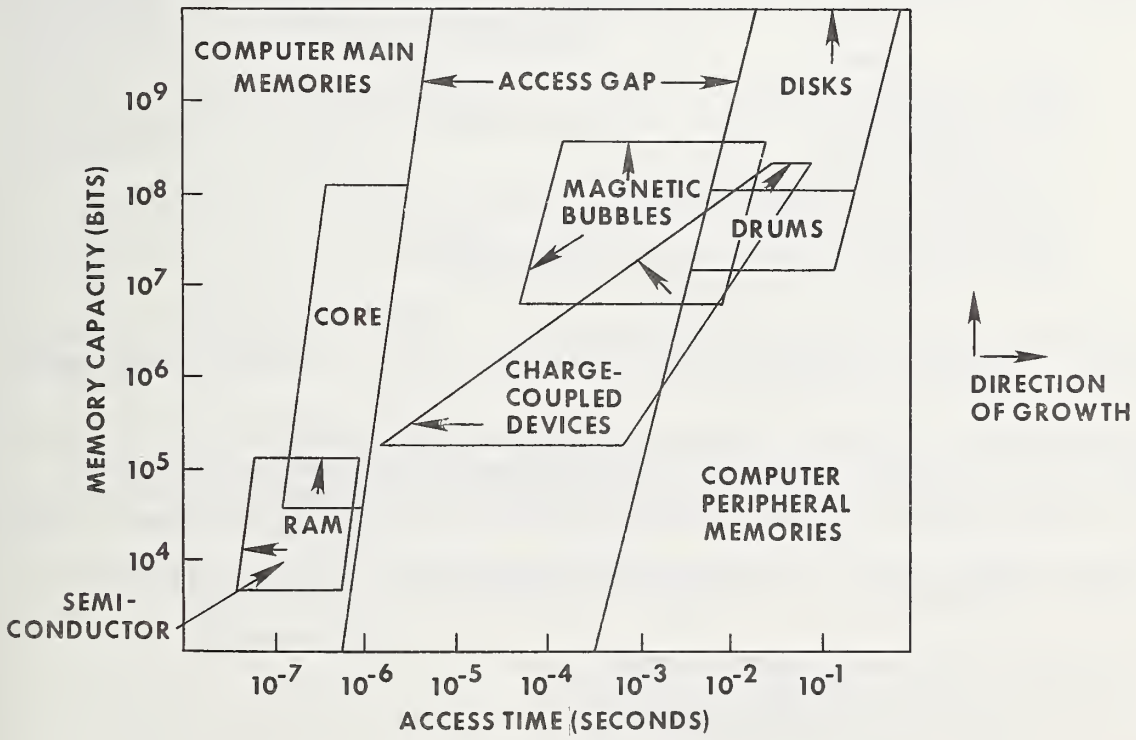

Figure 18: CCD Computer Memory Application Trends

CCD Computer Main Frame Memories

CCD memories cannot perform well in the computer main frame mode since CCD's are basically serial memories and therefore exhibit slow data access times. In order for CCD's to successfully compete with MOS or core random-access-memories (RAM), CCD memory access times should be between 0.1 and 1 microseconds with capacities of 10^4 to 10^8 bits, (see Figure 18). A serially arranged (major and minor loop design) CCD main memory of 10^6 bits with an average access time of 0.5 microseconds would require data to be clocked in the high gigahertz region. Hence, it is doubtful whether CCD's will replace conventional random-access computer main frame memories. [32]

CCD Computer Swap Memories

Application of the CCD in commercial computer swap memory is feasible today. Intel (U.S.) markets a one-million-bit CCD memory card which could serve very well as a computer swap memory when storing blocks of data from slow peripheral memories. The swap data can thus be block-random-accessed and can provide the computer main memory with its necessary data in shorter time intervals than the peripheral memories. [1]

Swap memories, currently used in advanced computer systems, are usually N-channel metal-oxide-semiconductor (NMOS) or P-channel metal-oxide-semiconductor (PMOS) solid-state memories. The replacement of these memories with CCD memories would be cost effective since CCD's are potentially less costly. Advanced fast CCD swap memories, operating at speeds greater than 100 MHz, could be built with capacities of $>10^6$ bytes and average access times of 100 microseconds and possibly even 10 microseconds. [40, 41]

CCD Computer Mass Memories
(Current and Future Designs)

CCD's are most likely to be accepted initially in computer peripheral mass memories as replacement for disk and drum peripheral memory units. Bell-Northern Research of Canada, a subsidiary of Northern Electric, built a CCD memory in 1975, to replace the DEC RS64 disk unit on a DEC PDP-11 Computer. Its operating characteristics are as follows: [52]

Capacity - 1 megabit
Number of words - 64,000
Access (latency) to any word - <200 microseconds, versus 11 milliseconds on the RS64 disk
Chip capacity - 8 kilobit CCD
Data organization - 256 bit blocks
Clocking rate - >800 KHz
System application - direct DEC RS64 replacement
System interface - PDP-11 Unibus

According to a Bell-Northern Research paper (see reference 63), the incorporation of the CCD disk replacement resulted in sizable reduction in power dissipation, and a marked reduction in latency over the RS64 disk.

The Bell-Northern CCD disk replacement memory bears similarities to a million bit CCD printed circuit card recently announced by Intel. However, the Intel product uses 16 kilobit chips as opposed to 8 kilobit chips in the Bell-Northern memory. Furthermore, Intel has announced the capability of producing 32 kilobit chips in the near future. [54]

Table 1 presents predictions make by a Bell Laboratory CCD scientist on the future development of CCD memories.

Table 1 - DEVELOPMENTS IN MEMORY CCD's (1975-78)

1. MINIMIZING CHIP AREA/BIT USING PRESENT DESIGN RULES

   (a) Use of SPS blocks (peripheral area savings over RAM.∿25%)
   (b) Use of interleaved parallel channels (50%)
   (c) Use of high density electrode structures or electrode/bit mode (∿50%)

   ∴ Packing density of memory CCDs ∿6 times higher than RAM for T_{Ac} ∿500 μs

2. IMPROVING ACCESS TIME

   (a) Use of faster peripheral circuits
   (b) Use of bulk channel CCDs
   (c) Small area, stable regenerators for serpentine organization

   ∴ T_{Ac} ∿10 - 100 μs

3. REDUCING POWER

   (a) Careful peripheral design
   (b) Lower dark current
   (c) Longer access times
   (d) Smaller cell sizes, lower voltages, thinner oxides

   ∴ Power ∿1W/MHZ/Mbit

4. HIGHER YIELD AND MORE BITS/CHIP

   (a) Simple electrode structures
   (b) Control of dark current
   (c) Electron beam fabricated masks
   (d) X-ray or electron lithography

   ∴ 64k or 128 kbit chips

5. MULTILEVEL STORAGE

   (a) Design of multilevel detection circuits
   (b) Control of dark current
   (c) Control of transfer inefficiency

   ∴ 256-512 kbit chips

6. NONVOLATILITY

   (a) Use of MNOS structure

   ∴ 16-64 kbit permanent memory chip

7. ADAPTIVE PROGRAMMING

   (a) Applicable to block addressed structures

   ∴ 256 kbit chips

Predictions made by M. F. Tompsett,
Bell Labs at the International Solid State
Circuits Conference
Philadelphia, Pa., February, 1975

2. CHARGE-TRANSFER DEVICE PARAMETERS

Bit-Storage Densities of Charge-Transfer Devices

In the silicon solid-state memory technology, bit-storage density of the charge-transfer device currently surpasses the densities of all other LSI silicon storage devices. At present, commercial products exhibit a chip-bit density of about 10^5 bits per square centimeter (about 10^6 per square inch). Initial CCD bit densities (in 1970) were about one order of magnitude lower and were found in chips with three orders of magnitude lower storage capacity than recent CCD's (see Figure 19). [24]

The CCD device development progress, from 16 bit chips with 10^4 bits per square centimeter to 16 kilobit chips with 10^5 bits per square centimeter (1975), in a period of less than five years, is impressive. It is anticipated that chips with 32- and 64 kilobit capacity and 10^6 bits per square centimeter will be marketed in the near future. [33, 54]

Charge-Transfer Efficiency of Charge-Transfer Devices

Since a charge-transfer device is comprised of a string of analog delay elements, each of which exhibits no gain, charge packet transfer occurs with certain losses. Such losses are expressed in percentage of charge-transfer efficiency. Charge-transfer efficiency directly influences the faithful reproduction of the processed signal. Regeneration of the deteriorated, transferred packets within the charge-transfer device is necessary since charge losses reduce the fidelity of the processed signal. Interstage amplifiers within the CTD must therefore be used if the register is long and the accumulated charge-transfer inefficiency interferes with the signal fidelity. On the other hand, it is important to minimize interstage signal regeneration since the additional diffusions (etc.) required for the amplifiers forces the use of more difficult fabrication techniques which can contribute to lower product yields. It is therefore extremely important to maximize transfer efficiency. [1]

Early CCD's, such as those produced by Bell Telephone Laboratories (1970), displayed typical charge-transfer efficiencies of 98%. This figure indicates an approximate 2% loss of charge per transfer. Rapid improvement in the CCD efficiency occurred from 1970 to 1973 and ratings of 99.9% efficiency are claimed by several U.S. manufacturers during this period. Hitachi, a Japanese firm, claims a 99.96% efficiency rating at 10 MHz operation. (The pairing of the efficiency rating and its operating frequency is very important since charge-transfer efficiency is highly frequency dependent and charge is lost faster at higher operating frequencies.) [55] (see Figure 20).

Currently, the most impressive charge-transfer efficiency ratings are those published by Philips in 1974 and 1975 articles which described the operation of a peristaltic charge-coupled device with efficiencies of 99.999% at frequencies of up to 180 MHz. [15, 56]

Charge-Transfer Device Data Rates

As shown in Figure 21a and b, data rates for bucket-brigade devices are generally slower than those for charge-coupled devices. In the period from 1971 through 1973, the data rates of BBD's and CCD's show an average speed of about 1 MHz per device. Some charge-transfer devices can be found that operate faster, but usually such devices are "tuned" laboratory models with low bit-storage capacities. [10]

A major breakthrough in CCD data rates occurred in 1974 when Philips introduced the peristaltic charge-coupled device which operates at speeds greater than 100 MHz and has the potential of gigahertz operation. [56]

According to Figures 21a and b, which were developed from information found in open literature, Fairchild Semiconductor, RCA, and Intel are the U.S. producers in high speed data rates for large capacity CCD's while Bell-Northern of Canada is the foreign producer in these respects. [52, 57]

BIT-STORAGE DENSITIES OF CHARGE-TRANSFER DEVICES

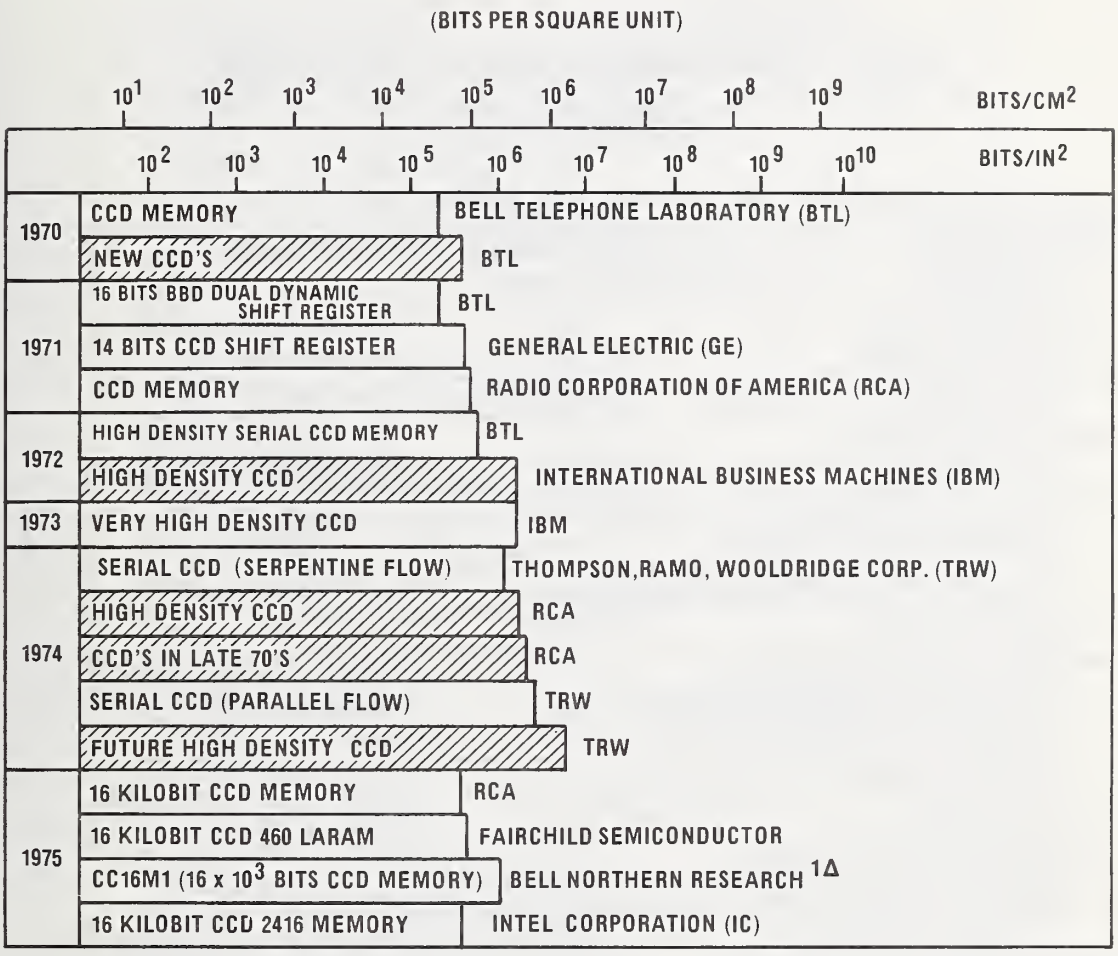

FIGURE 19

CHARGE TRANSFER EFFICIENCY OF CHARGE-TRANSFER DEVICES

(AT MAXIMUM OPERATING SPEED)

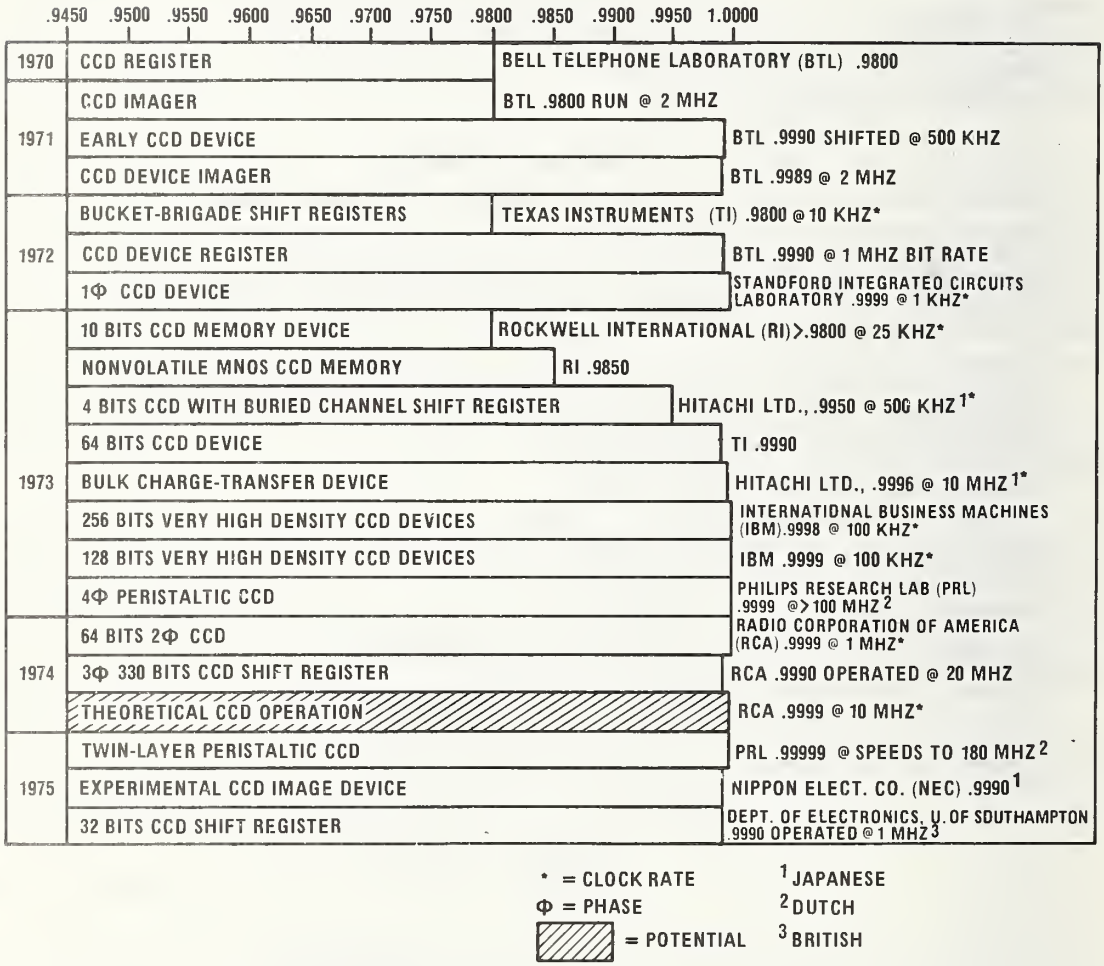

FIGURE 20

CHARGE–TRANSFER DEVICE DATA RATES

(@MAXIMUM HERTZ)

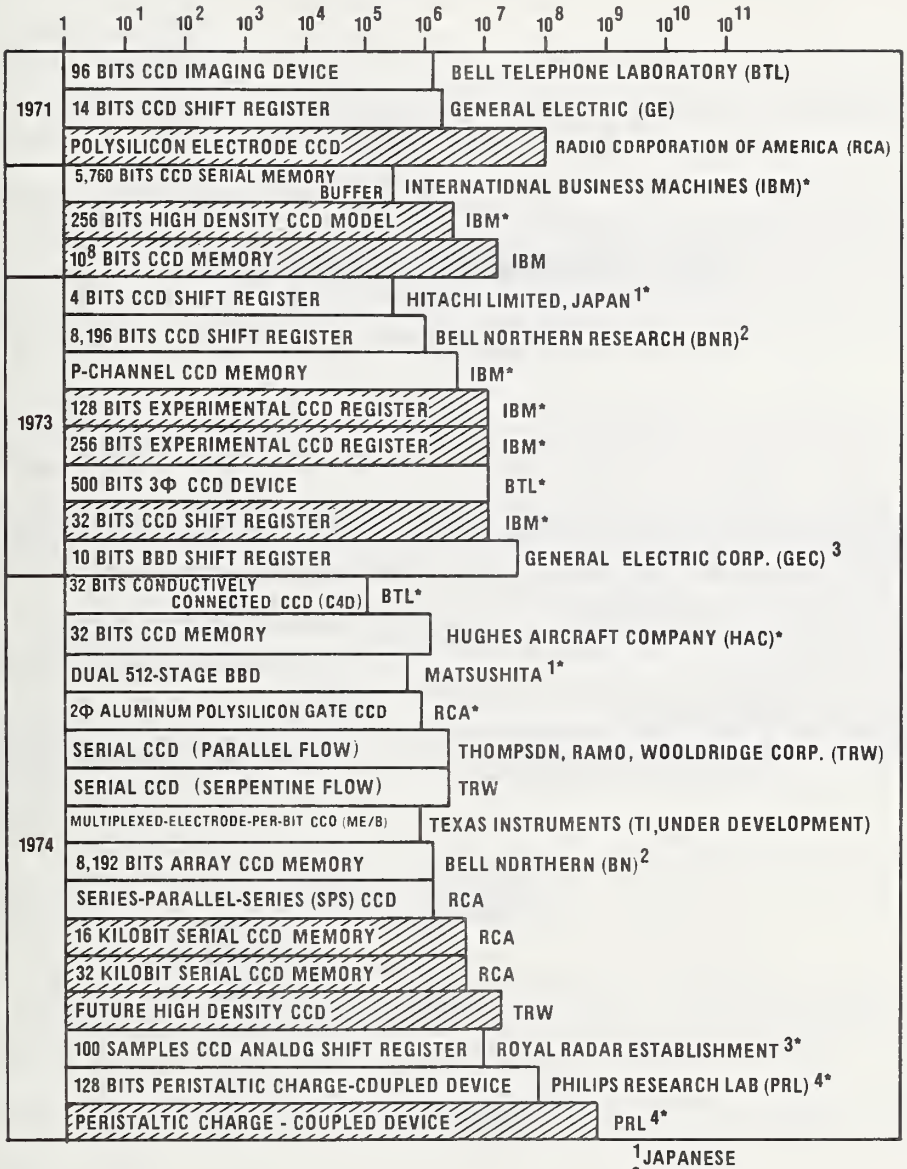

FIGURE 21a

CHARGE-TRANSFER DEVICE DATA RATES

(@ MAXIMUM HERTZ)

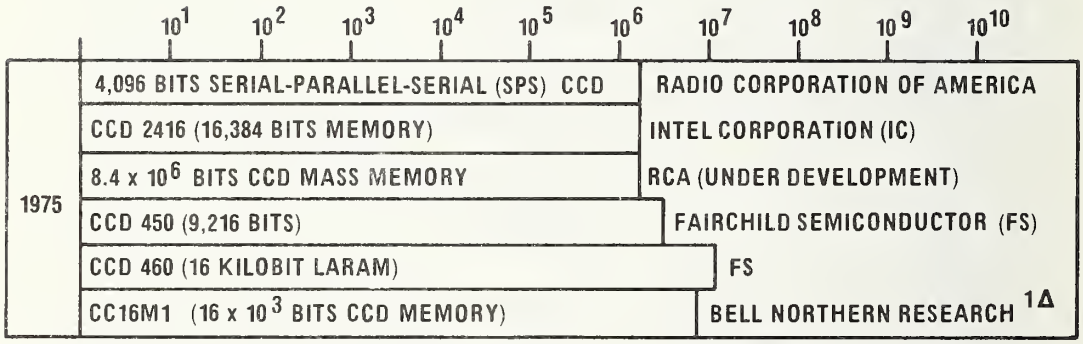

FIGURE 21b

Charge-Transfer Device Power Dissipation

Charge-transfer devices have very low power dissipation. However, power dissipation in CCD's must be measured under two conditions:

Standby Operation
Dynamic Operation

The difference between the above operating modes is that data are transmitted in the dynamic mode whereas the memory is idle under the standby mode of operation.

The standby power dissipation of CTD's usually does not vary, given that environmental conditions (temperature, humidity, power supply voltages, etc.) remain constant. The standby power dissipation of the CTD is always less than the dynamic power dissipation when measured under the same environmental conditions because the losses incurred in charging and discharging the MOS capacitors are frequency dependent. Since the CTD is operated at lower frequencies in the standby mode, relative to its dynamic operation, lower power dissipation is realized in this mode. [31, 58, 59]

In assessing the dynamic power dissipation, it is important to note the associated frequencies. Generally, the higher the frequency, the higher the dynamic power dissipation. Advertised CTD dissipation values usually assume some high frequency dynamic operation.

As shown in Figure 22, reported CCD and BBD power dissipation values range from approximately 0.1 microwatts to 10 microwatts per bit. It should be noted that the Matsushita BBD rating (1974) is given at a 10 KHz data rate operation while the CCD 460 from Fairchild Semiconductor (1975) is rated about the same at 5 MHz operation. The advertised BBD power dissipation is therefore only a relative value that can be expected to increase (probably drastically) when the unit is operated at higher frequencies. [21, 46]

Figure 22 shows that, of currently available devices, the lowest power dissipation occurs in the Fairchild, RCA, Intel, and the Bell Northern CCD products. These units dissipate about 10 microwatts per bit in the advertised operating modes. [54, 57]

Charge-Transfer Device Prices

Generally, the CTD price is highly dependent upon the quantity of devices being sold. The price of a single unit can be three or more times the price of single units that are bought in quantities of a thousand.

British and Canadian facilities were the first to offer commercial CCD's. The British unit (1974) is listed at a price of about 60 cents per bit in small quantities. Comparable U.S. units from Fairchild Semiconductor, like the CCD 201's can now be purchased at one tenth the British price, or about 6 cents per bit (see Figure 23). [60]

RCA currently advertises their SID 5000 series TV camera image sensors (512 x 320 bits) for about 1 cent per bit; the RCA price varies according to sensor quality (low or high blemish units). [61]

In the CCD memory market, Bell-Northern competes with the U.S. firms of Intel, RCA, and Fairchild Semiconductor. The Canadian firm charges of 0.1 cent per bit while Fairchild and Intel are asking 1 cent and 50 millicents per bit respectively. [41, 62]

It is anticipated that, if current trends continue, the CCD price could fall below the 10 millicents per bit in the near future. [40]

POWER DISSIPATION OF CHARGE–TRANSFER DEVICES

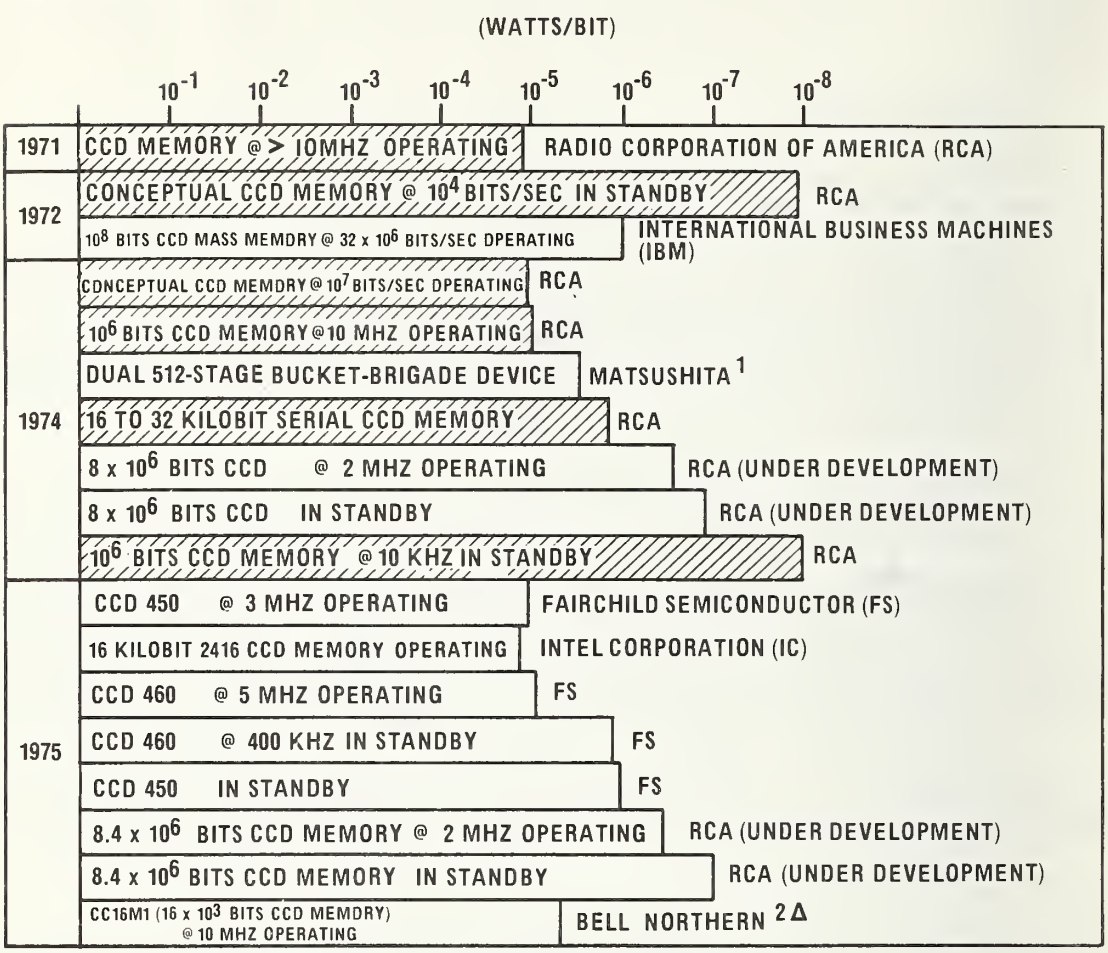

FIGURE 22

CHARGE-TRANSFER DEVICE PRICES

(CENTS/BIT)

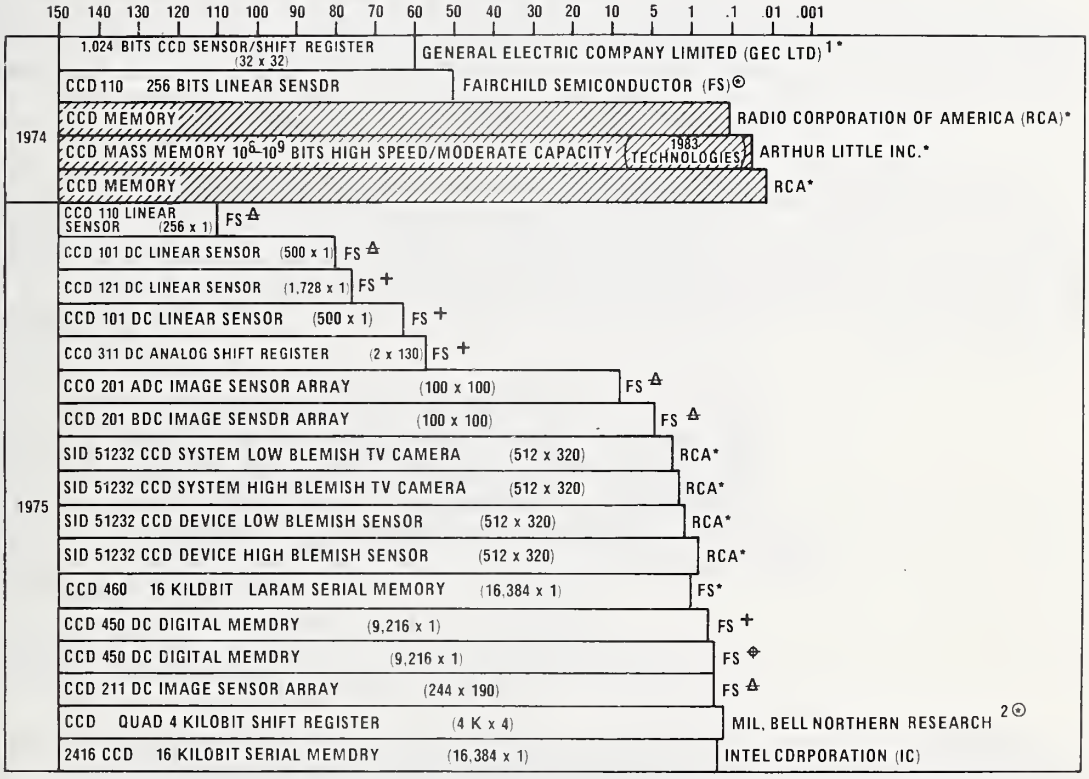

FIGURE 23

CTD Technology in Canada

Bell-Northern, a subsidiary of Northern Electric, is considered to be an important foreign competitor in charge-coupled devices. Bell-Northern, together with Microsystems International (both subsidiaries of Northern Electric), has recently produced commercial 16 kilobit CCD's with highly competitive features. [63]

Charge-coupled device research was pioneered by Canadian universities. The University of Toronto and Carleton University have experimented with CCD laboratory and mathematical models since 1973. Canadian scientists experimented with bucket-brigade devices, special metal-oxide-semiconductor transistors, and charge-coupled devices. [64, 65, 66]

Most experiments with the CCD's were aimed at improving high-frequency operation and device efficiency. High-frequency operation of the CCD is strongly related to the width of the interelectrode gaps of the device. Present photolithographic techniques allow fabrication of CCD interelectrode gaps that approach 2 micrometers. Smaller interelectrode gaps are difficult to fabricate since the limited resolution of the photolithographic process causes low product yield when such small gaps are required.

A significant breakthrough occurred when a process invented at Carleton University allowed the fabrication of 0.1 micrometer CCD interelectrode gaps. The Canadian process allows the fabrication of superior CCD's while utilizing conventional lithographic techniques. The process uses a castellated oxide structure which is held at an angle in a beam of aluminum atoms. Each raised (castellated) [66] structure provides the effect of a shadow, the width of which is controlled by the angle of incidence of the beam of aluminum atoms (see Figure 24).

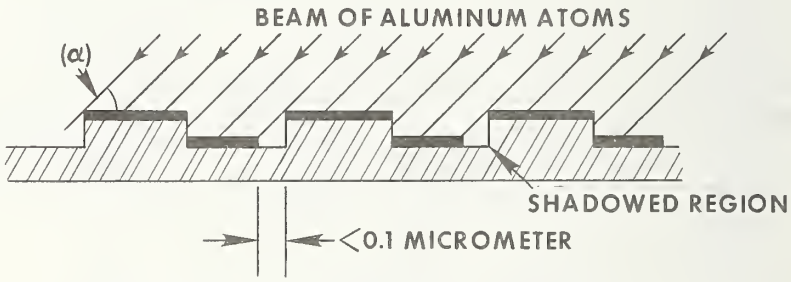

Figure 24: Castellated CCD Structure

Knowledge obtained from the various fabrication processes was applied to the production of 4- and 8 kilobit CCD shift registers. The shift registers are said to have "overlapping" gate structures. These structures combined with several "new techniques", according to Bell-Northern, were implemented in memory chips that were considerably smaller than other CCD memory chips of the same capacity. [52, 63]

The new Bell-Northern 16 kilobit device is capable of operating at 10 MHz data rates. At the same time the unit offers extremely low operating and standby power dissipation. [63]

CTD Technology in The Netherlands

Philips, the Dutch electronics firm, is making important contributions to CCD technology. In order to substantiate the commitment of the Philips facilities, the following events are presented as indicators:

Invention of the BBD

F. L. J. Sangster, a Philips scientist holds the patents of this device. The BBD is the predecessor of other charge-transfer devices (CTD's), such as the charge-coupled device (CCD). [6, 67]

Invention of Integrated Injection Logic (I^2L)

Philips developed I^2L simultaneously with IBM in Germany. I^2L offers several advantages over current LSI circuits (TTL, NMOS, etc.) in the form of greater bit density at higher operating speeds. [68]

Invention of the Peristaltic Charge-Coupled Device (PCCD)

L. J. M. Esser, another Philips scientist, invented this type of charge-coupled device. The PCCD presently operates more efficiently and at much higher frequencies than conventional CCD's or BBD's. [56]

Entrance into the Complementary-Metal-Oxide-Semiconductor (CMOS) Market

Philips recently produced a highly competitive CMOS product line using a proprietary local oxidation process to build standard CMOS devices. According to Philips, the new CMOS line has three to five times the performance potential of standard CMOS. [69]

Merger of the U.S. firm Signetics with the Worldwide Philips Organization

The acquisition of the Signetics facility by Philips provides the Dutch corporation with two significant advantages: [70]

1. N-channel metal-oxide-semiconductor (NMOS) knowledge (much U.S. silicon LSI circuitry is now NMOS and Signetics has a strong position in NMOS technology).

2. Mass production capability located in the U.S.

As early as 1965, Philips was involved in MOS transistor improvement studies. [71] Philips was the first corporation to offer a commercial BBD, called the M31. It is available through the Philips outlet Amperex, according to an advertisement in Electronic Design. [45] BBD's are also used in a relatively new variable speech control system (VSC). The VSC system allows a two-hour recording to be compressed into less than 45 minutes. The BBD is designed as an audio delay line into a system, the operation of which results in normal speech reproduction over a wide range of playback speeds. [45]

Since the invention of the CCD by Bell Telephone Laboratories, Philips has produced new BBD products. One of the first products which was tried was the TETRODE BBD (TBBD). The TBBD was designed as an audio delay line with very low distortion. A unique 512-stage device was built on a 3 x 3 millimeter chip. The distortion of the device response was about 5% at a data bandwidth of about 10 kilohertz. [72]

Another product announced recently features a 512 bit BBD with a 5 to 500 kilohertz operation. The unit, called a TDA 1022, operates over a temperature range of -20° to +55°C. The product is aimed at the commercial recording market for possible use in variable speed control or speech compression circuits. [67]

Another Philips invention is the peristaltic charge-coupled device (PCCD). It is said to have higher frequency operating characteristics than either the BBD, the TBBD, or the conventional CCD. However, PCCD's are not yet commercially available. [73]

Conventional charge-coupled devices are speed limited since the individual charge packets fail to transfer as a whole at high frequencies. Mobile charge carriers, which are left behind, cause distortion in transferring packets. Peristaltic charge-coupled devices are designed such that fewer charge carriers are left behind from the packet that is being transferred. The new Philips design has the potential of operating one hundred (100) times faster, at comparable or greater charge-transfer efficiencies, than conventional charge-coupled devices. Presently, all literature found on PCCD design indicates that Philips is the sole source of this product. [15]

Leonard J. M. Esser, inventor of the PCCD, expects that his invention will eventually operate in the gigahertz region. [56] If the PCCD is indeed capable of stable operation at gigahertz frequencies, then the device could cause a revolution in modern day radar system design by using the PCCD's as high frequency filters in radar receivers. This design should be vastly superior to current radar designs. [56]

Indications are that the U.K. Royal Radar Establishment is buying some Philips products for their experimental radar systems. Some sources state that the British (early pioneers in radar) have made several major breakthroughs in moving-target-indicator filter designs. [42]

Table 2 shows the Dutch devices and products from the U.S. market. Signal processing CTD's can be reorganized in this table since they excel in either high transfer efficiency or high speed. On the other hand, memory and image sensor CTD's exhibit characteristics such as high bit-storage density. A comparison of the various CTD products reveals that Philips charge-transfer devices are primarily aimed at the signal processing market whereas the U.S. CCD's are usually for use as memory and image sensor devices. In addition, the table shows that the Philips products address the signal processing market with devices which exhibit higher frequency operating characteristics than any other charge-transfer device.

Table 2 - Charge-transfer Device Technological Accomplishments in The Netherlands and the United States

	Products	Materials	Bit Storage Capacity	Operating Temperature Range	Operating Frequency Range	Device Charge Transfer Efficiencies	Commercial Packaging Techniques	Product Applications	Price
The Netherlands	BBD's CCD's and PCCD's	Silicon with phosphorus or arsenic ion implantation and aluminum metalization.	Relatively low bit density (not memory oriented)	BBD's @20°C to 50°C PCCD's--(no temperature data were given)	BBD's @5-500 kilohertz PCCD's @potential gigahertz operation	PCCD's @ 180 MHz-99.999% (S/N of 80dB)	Dual-in-line (DIP) or similar packages	BBD's for audio signal processing. PCCD's for radar, television, communications, and instrumentation. (No imaging devices found)	$4 to 10 each in BBD's (Mass quantities)
United States	CCD's	Silicon with phosphorus or boron ion implantation and aluminum metalization	High bit density (10^6 bits per square centimeter)	CCD's @0°C to 70°C	CCD's @20MHz	CCD's @ 20 MHz-99.999% (S/N of 60dB)	Dual-in-line (DIP) packages	CCD's for television imaging, audio recorders, and memories	$9 to several hundred dollars each in CCD's. (Mass quantities)

CTD Technology in Japan

The approach by Japanese firms towards charge-transfer technology appears similar to that of Philips. However, dates of articles indicate that the Japanese firms have been involved in the charge-transfer technology for a period of less than five years, whereas Philips articles date back at least six years. [55, 74, 75]

The Japanese experiments pursue the usual goals of high frequency operation, high charge transfer efficiency, and high bit-density. Japanese research facilities presently engaged in charge-transfer device research include the following:

Hitachi Ltd. [55]
Matsushita Electronic Corporation [76]
(Panasonic)
Tokyo Shibaura Electric Co., Ltd. [77]
(Toshiba)
Nippon Electric Co., Ltd. [75]
(NEC)

In 1972, Hitachi fabricated a charge-coupled device by a unique technique. They implemented a buried-channel CCD structure (similar to the Philips approach) fabricated with nonoverlapping gate electrodes (unlike the current Bell Northern approach). The units were ion-implanted with boron (unlike Philips, which uses phosphorus and arsenic, but more like the U.S. approach). The experimental four-bit, three-phase CCD did not exhibit outstanding physical or operational parameters. The interelectrode gap lengths were 6 micrometers (versus Bell-Northern's 0.1 micrometer). The high frequency operating range was a low 500 KHz with a moderate 99.5% efficiency. However, these were 1972 results. [74]

Little charge-transfer device activity was reported in technical literature in the period between 1972 and 1974. However, late in 1974 Electronic News carried Matsushita's announcement of their commercial bucket-brigade device. The commercial BBD, model MN3001, was placed on the market in November 1974. Specifications supporting the MN3001 claim an 800 KHz clocking rate and a 70dB signal-to-noise ratio. These are quite respectable operating parameters. Matsushita plans an initial production level of 10,000 BBD's a month, but the anticipated maximum output is reported to exceed 100,000 units a month, [46, 76]

The rate of progress of silicon technology in Japan in the development of charge-transfer devices is indicated by a report in Journal of Electronic Engineering (Japan). According to the article, Panasonic plans to introduce the Japanese BBD into a variety of applications, such as: [46]

Variable Speech Control (VSC)
Voice Control of Tape Recorders
Reverberation Designs in Stereo Equipment
Tremelo, Vibrato, and Chorus Effects in Musical Instruments
Variable or Fixed Delay Lines for Analog Signals
Telephone Signal Time Compression and Voice Scrambling in
Communication Systems

NEC has also successfully developed a CCD imaging/memory device. It includes an imaging array of 64 x 64 elements and a storage unit of 64 x 68 elements. Stored data are transmitted via a CCD shift register which consists of 69 stages. The imaging/memory unit has marked similarities to other designs such as the Fairchild CCD imaging device which was developed earlier in the U.S. [75]

Japanese companies have also adapted CCD's to their color cathode ray television tube (CRT) instrumentation equipment. Units described in the Japanese trade press are reportedly being used as variable delay lines in TV convergence alignment systems. Tokyo Shibaura Electric Co. (Toshiba), produced a 64 bit CCD shift register which is said to operate beyond the 20 MHz frequency range (the approximate limit of U.S. CCD device operation). The Toshiba CCD Variable Delay Line (VDL) system delivers convergence quality superior to that obtained by conventional methods. [77]

In general, it appears that charge-transfer devices were first produced in Japan by using knowledge transferred from foreign sources. Later models are using increasingly unique and original methods. Products such as BBD's and CCD's are supported by specifications which could be highly competitive with any CTD manufacturer's products.

The Japanese-manufacturered CTD products are generally not aimed at the computer memory market. Most applications found in this survey placed these CTD products in the "small electronic machine" category, which includes such devices as tape recorders, audio equipment, and television cameras. [46, 77]

Once a CTD product application appears successful, the Japanese semiconductor manufacturers apparently have no problems in mass producing large quantities of the electronic devices.

CTD Technology in Great Britain

British Scientists have long been interested in charge-transfer devices. Early charge-transfer device experiments by the Royal Radar Establishment (RRE) used BBD's as delay lines in radar designs. [42, 43] Several British universities and corporations are pursuing charge transfer research in conjunction with Canadian firms, and commercial CCD products have been marketed by British companies. Some of the facilities prominent in British CTD investigations are: [66]

Royal Radar Establishment - CCD experiments (in radar and television design) [42, 43]
GEC Semiconductors Limited - CCD product applications (imaging/memory and delay lines and radiation experiments)
University of Edinburgh - CCD experiments (math and lab models) [78]
Univeristy of Liverpool - Nonsilicon CCD experiments [79]
School of Electronic Engineering Science (Wales) - CCD experiments (CCD bonding and fabrication techniques) [17]

In general, most British charge-transfer device development is oriented toward advanced radar systems rather than computers. Little mention of memory application of the charge-transfer device is found in the literature, although British research facilities have used CTD shift registers for various other applications.

In 1973, RRE developed a moving-target-indicator (M.T.I.) filter with the M31 Philips bucket-brigade shift registers. This filter, when used in conjunction with a radar signal, discriminates between the returns from stationary objects and those from moving objects by comparing a "memorized," or previously returned radar signal with the presently returned signal. The comparison of the two returns results in cancellation of returns from fixed objects. This technique is used in many radar systems to prevent the display from being cluttered by large echo signals produced by terrain features. [42]

The British MTI experiments showed that the BBD's could not be clocked faster than 100 KHz, which resulted in a distance resolution of only 1.5 kilometers for the experimental radar equipment. However, later experiments used an improved MTI filter with a 330 KHz clocking capability and 99.90% transfer efficiency resulting in a direct increase in range and clarity of the display signal. [43]

Dr. Roy Eames, an RRE CCD specialist, has predicted that radar MTI designs are likely to be the first application of the CCD shift register. He states that the present 100 millisecond delay, 40 dB dynamic range, storage capacity of 100 samples, clock rates of greater than 10 MHz, and simple serial access to data, makes the CCD ideal for radar MTI signal processing designs. [80]

Dr. Donald J. MacLennan of the University of Edinburgh, formerly an RRE scientist, has developed a unique technique to tap the analog signal nondestructively as it is passed along from one cell to another. Dr. MacLennan claims that the tapping, with the shift registers in parallel, uses the entire available system bandwidth, which promises to triple the data rate now achievable only with complex three-phase CCD's. Moreover, the tapping design may eliminate sample-and-hold circuitry in some applications. [78, 80]

Recent British experiments in CCD's show trends towards improving CTD fabrication methods. One method, proposed by the University of Liverpool, suggests an experimental gallium arsenide (GaAs) CCD. The goal of the design was to fabricate a CCD laboratory GaAs model with practically zero interelectrode gap distances. The zero interelectrode gap distance criterion is impossible to meet in silicon with the use of conventional lithographic techniques. The GaAs technique is novel and has the potential of extremely high frequency operation. [79, 81]

Late in 1974, GEC Semiconductors Limited, announced their CCD product, the CD200, at a cost of $600 each. The 32 x 32-bit metal gate N-channel MOS charge-coupled device uses a serial-parallel-serial mode of operation. The result is reduced degradation of the analog signal and shorter delay times for digital words. Recently produced U.S. CCD's operate by similar principles as the CD200. [60]

CTD Technology in the Federal Republic of Germany

Articles in open literature indicate that bucket-brigade research activity in Germany was underway in 1973. An AEG-Telefunken scientist, W. Frey, reported the computer simulation of an "improved" BBD shift register. The computer model implemented one additional transistor and one "ohmic resistor" per cell as an effective means to reduce the charge-transfer inefficiency of the BBD. [7]

The computer simulation indicated improved frequency operation due to a more complete transfer of charge from one cell to the next. Operation of 10 MHz (versus the then usual 100 KHz limit) was found feasible, but only at the cost of doubling the chip area. No products implementing the described method have been reported in German literature. [7]

Siemens' literature presented at the International Conference in Edinburgh (1974), included a nonvolatile CCD memory design. The memory, developed by German scientists, introduced the metal-nitride-oxide semiconductor (MNOS) capacitor in a CCD memory in order to achieve nonvolatility of data storage (U.S. Patent Numbers 3,508,211 and 3,590,337; R. Wegener). Supporting technical data suggests that the CCD MNOS memory design is far from primitive. Deposited oxides of SiO_2 and Si_3N_4 were 20 angstroms thick which is comparable to U.S. technology limits. The laboratory model combines the advantage of the high packing density of the CCD with the nonvolatility of MNOS circuits. However, the nonvolatility is achieved at the expense of device packing density since the MNOS capacitors demand a great deal of chip area. No indication is given as to how long data can be stored in the CCD/MNOS memory. (Nonvolatility of MNOS stored data is time dependent in that the charge on the oxide capacitors depends on the length of read-in time and the number of read-out cycles. The CCD/MNOS memory, therefore, exhibits conditional long-term retention of stored data rather than pure unconditional nonvolatility of data storage. Long-term conditional retention is not as desirable as the nonvolatile characteristic shown by magnetic core or magnetic bubble memories which store their data indefinitely.) Perhaps the principal point to be derived from the revelation of the CCD/MNOS memory design is the ability of the German facilities to produce sophisticated CCD memories. [29]

4. SUMMARY AND CONCLUSIONS

Information found in both non-U.S. and U.S. literature indicates that two types of charge-transfer devices are currently produced--the bucket-brigade and the charge-coupled device.

The bucket-brigade device was invented first and it differs in construction from the charge-coupled device. Manufacturers of bucket-brigade devices form impurity wells in their products for charge storage whereas charge-coupled devices depend upon electric potential wells without doping. In general, the application of the bucket-brigade was found in low frequency designs such as audio delay lines in audio systems. In some instances, however, the application of the bucket-brigade was described when functioning in radar systems. The literature revealed that many of the bucket-brigade units are produced by non-U.S. manufacturers. Particularly manufacturers in The Netherlands and Japan are producers, although lately a few U.S. sources are also advertising BBD's.

Articles in the available literature on charge-coupled devices indicate that these devices are researched vigorously in both U.S. and non-U.S. research facilities. Applications of CCD's as described in the literature were exceedingly diverse.

Most digital applications of the CCD's were found to be in volatile memory systems. Current advertisements show that digital storage capacity of the CCD has reached about 16,000 bits per chip with associated data rates of over 10 MHz. Peristaltic CCD's, described in articles from a research facility in The Netherlands, operate as high as 180 MHz with better than 99.999% efficiencies. Predictions of gigahertz operation accompanied such information. The combination of high-speed digital operation with large bit-storage per chip was generally found to exist in products from the U.S. or Canada while lately some from Great Britain were also noticed. High-speed CCD units with high-efficiency operation were often described in literature from The Netherlands. Nonvolatile digital memory operation has been accomplished by both U.S. and non-U.S. facilities. West German researchers have published articles that describe how metal-nitride-oxide semiconductor material was successfully implemented with CCD memories in order to obtain memory nonvolatility.

In the analog field, many described applications are image sensors, delay lines, and signal processors (filters, etc.). Activity in CCD sensor, or image, research was found primarily in facilities located in the United States, Great Britain, and Japan. Many of these facilities apply their CCD sensors to television cameras as substitutes for the vidicon tubes. Manufacturers of television equipment in Japan report that CCD sensors are used in instrumentation to facilitate and thereby speed-up the production of television sets.

The application of CCD's to radar systems (moving-target-indicator filters) has produced significant results by clearing up unwanted clutter in radar displays. Literature indicates that radar research with CCD's is conducted by the Royal Radar Establishment in Great Britain.

Table 3 is constructed from data found in available published information. The table allows a comparison of technical accomplishments in the field of charge-transfer devices. The realization that charge-transfer devices are here, are available, and are being implemented into a variety of electronic systems is reflected by this table and a list of products published in a current magazine. [82] The list reveals that charge-transfer device application is directed mainly toward three areas. These areas are:

Computer memory
Image sensing, storage, and transmission
Both analog and digital data processing

Table 3
Technological Accomplishments of Non-U.S. and U.S. CTD Facilities
(Through 1975)

Location of Facilities	Materials	Device Applications	Data Storage Capacity	Charge-Transfer Device Type	Charge Transfer Efficiency (CCD's)	Frequency Range	Interelectrode Gaps in Micrometers	Commercial Packaging
United States	Silicon	Memories, sensors, & filters	Up to 16 kilobits in CCD's	CCD's	99.990%	20 MHz	0.25	Dual-in-line @<$16
Canada	Silicon	Memories (DEC, RS/64 Disk Replacement) and sensors	Up to 16 kilobits in CCD's	CCD's & BBD's	99.990%	>10 MHz	2-3	Dual-in-line @ $30
The Netherlands	Silicon	Delay lines and data processing devices	Up to 512 bits in BBD's and 128 bits in PCCD's	BBD's & CCD's	99.999%	180 MHz	2	None found
Japan	Silicon	Sensors, delay lines, & instrumentation	Up to 1024 bits in BBD's, 64 x 64 bits in sensors	BBD's & CCD's	>99.980%	>10 MHz	3	None found
Great Britain	Silicon & Gallium/ Arsenide	Radar filters and sensors	1024 bit sensor memory and delay line; radar filter	CCD's	>99.900%	>1 MHz	0.5-2	Dual-in-line or similar package @ $600
The Federal Republic of Germany	Silicon with MNOS capacitors	Memories with nonvolatility	128 bit MNOS/ CCD non-volatile memory	CCD's with MNOS storage	None found	None found	5-6 in MNOS/CCD design	None found

In reviewing the numerous articles on which this report is based, it was found that computer memories and televison cameras (sensors) are the primary areas of application for charge-coupled devices, whereas the area of signal processing appears to be addressed by both CCD's and BBD's.

Competition between CCD memory products and several conventional memory technologies is evident throughout most of the reviewed literature. One large solid-state product manufacturer [83] is including CCD memory cells in their soon-to-be-announced 16 kilobit RAM memory. Another manufacturer [84] has the following expectations:

65 kilobit CCD by the end of 1976
128 kilobit CCD within the next two to three years
400 to 500 kilobit CCD's with the use of electron beam lithography.

The latter manufacturer also offers a complete television camera system that uses charge-coupled device sensors. [85] The article states that the camera operates with standard closed-circuit television and video recorders, is small size, light weight, low power and exhibits long life when compared to conventional tube type imaging sensors. Other facilities have produced similar devices [35, 61] and their literature and advertisements indicate an eagerness to enter into the fast-growing solid-state image sensor market.

BBD's and CCD's are currently being used as signal processors in radar and audio applications. But, when this activity is compared to the efforts found in CCD memory and image sensing literature, CTD signal processing products appear to address only minor markets. It is difficult to determine the cause of this slower development especially since the CCD exhibits relatively superior characteristics when used as a logic element.

T. A. Zimmerman [86] points out in one of his technical papers that CCD's exhibit a ten to one advantage in both device bit-storage density and speed-power product when compared to characteristics of competing devices. He further adds that CCD's were initially perceived as analog devices and very few facilities recognized the aforementioned digital advantages. According to Zimmerman, flexible, programmable digital CCD devices, directly interfaceable with the currently available large CCD memories, can presently be built. Computing systems, comprised of such CCD logic [86], large CCD memories, and efficient CCD image sensing and storage systems, could exhibit highly competitive features over existing computers.

Even though such systems can be built today, says the author, the success of such venture appears to be primarily a function of consistent investment in digital CCD research and development.

5. GLOSSARY

Glossary Terms Applicable to Charge-Transfer Devices*

1. Background Charge - Synonym for circulating bias charge used mainly in imaging devices.

2. Bucket-Brigade Device - A charge-transfer device that (1) stores charge as majority carriers in doped regions in the surface of a semiconductor that become reverse biased with respect to the substrate and (2) transfers this charge as a packet along the surface through a series of switching devices that interconnect the doped regions.

3. Bulk-Channel Charge-Coupled Device (BCCD) - A synonym for buried-channel charge-coupled device.

4. Buried-Channel Charge-Coupled Device (BCCD) - A charge-coupled device that confines the flow of charges to a channel lying beneath the surface of the CCD.

5. Charge-Coupled Device (CCD) - A charge-transfer device that stores minority carriers in potential wells and transfers this charge as a packet by translating the potential minima parallel to the device surface.

6. Charge-Coupled Image Sensor - A charge-coupled device in which an optical image is converted into packets of charge that can be transferred as the electrical analog of the image.

7. Charge Packet - A quantity of electrical charge that is the sum of the signal charge and bias charge (if used) and is stored in potential wells.

8. Charge-Transfer Device (CTD) - A device in which operation depends on the movement of discrete packets of charge along or beneath the semiconductor surface.

9. Charge-Regeneration Stage - A region of a charge-transfer device that is used to refresh digital information stored in a bit location.

10. Circulating Bias Charge - A quantity of electrical charge that is inserted into the potential well to define the low charge level.

11. Conductivity-Connected Charge-Coupled Device (C^4D) - A charge-coupled device that uses doped regions between the potential wells and hence becomes a hybrid between a charge-coupled device and a bucket-brigade device.

12. Drift-Aiding Fringing Field - An electric field at the semiconductor/insulator interface along the direction of charge propagation due to the potential of adjacent gate electrodes and the potential on the gate electrode directly above.

13. Empty Zero - A condition where there is zero circulating bias charge.

14. Fat Zero - Synonym for circulating bias charge that is used mainly in digital devices.

15. Floating Diffusion - A diffused area into which a charge packet can be introduced, thereby changing its potential; typically used in detection or regeneration schemes.

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* Most of the presented glossary was extracted from material published by the Electron Device Engineering Councils (EDEC Solid State Products Council Report, June 17, 1975).

16. Floating Gate - An electrically floating plate (pad) that is on an insulating surface over an active portion of the semiconductor surface; typically used in detection or regeneration schemes.

17. Gate Electrode: Transfer Electrode - A plate (pad) that is on an insulating surface over an active portion of the semiconductor surface and to which potential is applied.

18. JFET Bucket-Brigade Device (JFET BBD) - A bucket-brigade device in which the switching devices are junction-gate field-effect transistors.

19. Junction-Gate Charge-Coupled Device - A buried-channel charge-coupled device that uses a diffused junction as the gate electrode.

20. MOS Bucket-Brigade Device (MOS BBD) - A bucket-brigade device in which the switching devices are MOS field-effect transistors.

21. Multiphase Charge-Coupled Device - A charge-coupled device that requires more than one clock for operation of the device.

22. N-Channel Charge-Coupled Device - A charge-coupled device fabricated so that the charges stored in the potential wells are electrons.

23. Overlapping Gate Charge-Coupled Device - A charge-coupled device formed so that adjacent gate electrodes overlap and are insulated from one another.

24. Peristaltic Charge-Coupled Device - An advanced form of a PCCD that depends upon complex multilayer surface isolation techniques for operating in the high-frequency region with extremely high efficiency.

25. P-Channel Charge-Coupled Device - A charge-coupled device fabricated so that the charges stored in the potential wells are holes.

26. Potential Minimum - A local minimum of the electrostatic field.

27. Potential Well - A spatially defined depletion region of a charge-coupled device where the potential minimum exists.

28. Schottky-Barrier Charge-Coupled Device - A buried-channel charge-coupled device that uses a Schottky barrier junction as the gate electrode.

29. Signal Charge - A quantity of electrical charge in a potential well that, in conjunction with the bias charge (if used), defines the signal level.

30. Surface-Channel Charge-Coupled Device (SCCD) - A charge-coupled device in which the potential wells are created at the semiconductor-insulator interface and charge is transferred along that interface.

31. Transfer Channel - The area of a charge-coupled device in which the charge flow is confined. Note: This is physically accomplished by means of an oxide step, a channel-stopping diffusion or implant, or by a special edge-guard electrode.

32. Uniphase Charge-Coupled Device; One-Phase Charge-Coupled Device - A charge-coupled device that has asymmetric wells so that only a single clock is necessary to transfer the charge in the desired direction.

Glossary of Memory Terms

1. Access Time - The time between input memory addressing and output information availability
2. Bit Density - A measure of the number of bits stored per unit of length or area in the storage medium.
3. Cache - A high-speed memory whose contents are continually updated in blocks from a larger, slower memory to make the effective memory access time approach that of the higher speed (cache) memory.
4. Charge-Coupled Device - A semiconductor device which propagates signals by the movement of charge packets.
5. CMOS (Complementary-Metal-Oxide-Semiconductor) - Circuitry and logic employing both P-channel and N-channel MOS transistors with opposite, or complementary, switching characteristics.
6. Latency - A delay time in accessing information from a storage device.
7. LSI (Large-Scale-Integration) - A silicon (or other material) chip containing many gates.
8. MOS (Metal-Oxide-Semiconductor) - A field-effect transistor where the gate is insulated from the channel between source and drain by a metal oxide.
9. RAM (Random-Access-Memory) - A memory capable of being addressed in any sequence for either reading or writing.
10. Semiconductor Memory - A memory whose basic storage elements are semiconductor devices.
11. TTL (Transistor-Transistor Logic, or T^2L logic) - A standard integrated logic structure consisting of interconnected transistors.
12. Volatile Storage - A memory device which loses data when power is removed.

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16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

This document assesses the status of charge-transfer device technology as displayed by foreign research and manufacturing facilities for a period up to September 1975. Capabilities and accomplishments of charge-transfer device research facilities in Japan, Canada, Great Britain, The Netherlands, The Federal Republic of Germany, and the United States are described. Technical and economic factors are addressed and compared. Conclusions are presented which suggest future impacts of charge-transfer devices on current electronic systems, especially computers. Information contained in this report was derived from the open technical literature and from interviews with various U.S. technical experts. The technology assessment resulting in this report was conducted by the Information Technology Division of the Institute for Computer Sciences and Technology, National Bureau of Standards, as part of an " Advanced Computer Technology Survey" project.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Bucket-brigade; buried channel; Canada; charge-coupled device; Great Britain; imager CCD's; Japan; peristaltic CCD's; surface channel; The Federal Republic of Germany; The Netherlands; transfer channel

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